CLAIMS

What is claimed:

1. A computer peripheral device comprising:

    a memory for storing a configuration address; and

    a power level control circuit for controlling the power level in the device, the circuit being couple to the memory to cause the memory to store the configuration address from a bus when the device enters a normal power mode.

2. The device defined by claim 1 wherein the memory, once storing a configuration address, retains that address until the device is reset or power is turned on or off.

3. The device defined by claim 2 wherein the memory does not change its stored address when the device is reconfigured.

4. The device defined by claim 3 wherein the bus is an address bus.

5. The device defined by claim 4 wherein the memory restores an address after a reset signal is received by the circuit or power is turned on or off.

6. The device defined by claim 5 wherein the circuit is responsive to two addresses once a configuration address is stored.

7. The device defined by claim 1 wherein the memory restores an address after a reset signal is received by the circuit or power is turned on or off.

8. A computer system comprising:

    a processor; and

a plurality of peripheral devices coupled to the processor through at least one bus, each device having a power level control circuit and a storage circuit for storing a configuration address, the storage circuit storing a configuration address from the bus when the power level control circuit initially powers up the device in a normal operating mode.

9. The system defined by claim 8 wherein the bus is an address bus.

10. The system defined by claim 8 wherein each of the peripheral devices are initially sequentially brought into a normal operating mode from a standby mode.

11. The system defined by claim 10 wherein the peripheral devices are sequentially powered up after a reset or after power is turned on or off.

12. A computer system comprising:

a processor;

an output unit coupled to the processor; and

a plurality of peripheral devices each being coupled to a bus and each being coupled to a power level control line from the output unit, each peripheral device having a memory which receives and stores a configuration address from the bus in response to a signal on its respective power level control line causing the device to enter a normal operating mode.

13. The system defined by claim 12 wherein the bus is coupled between the output unit and the peripheral devices.

14. The system defined by claim 13 wherein the bus is an address bus.

15. The system defined by claim 12 wherein the memory of each of the peripheral devices store a configuration address only when first entering the normal operating mode after a reset or after power is turned on or off.

16. A method for operating a computer system comprising:

sequentially entering a normal mode from a standby mode for each peripheral device; and

storing a unique configuration address is each device as each enter the normal mode.

17. The method defined by claim 16 wherein the storing step occurs after reset.

18. The method defined by claim 17 wherein the storing step for each peripheral device includes the reading of data from a bus.

19. The method defined by claim 18 wherein the reading of data from a bus comprises the reading of data from an data bus and an address from an address bus.

20. The method defined by claim 18 including configuring each peripheral device after it has stored its configuration address.